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(54) Title: METHOD TO DECREASE DISHING RATE DURING CMP IN METAL SEMICONDUCTOR STRUCTURES

(57) Abstract

A method for reducing the rate of dishing or erosion of composite semiconductor structures containing at least two different films is provided. Most preferably, the structure consists of a metal layer, a dielectric layer, and a barrier layer. The method compries planarizing a composite semiconductor structure with a polishing slurry and a polishing pad having a planarizing surface. By minimizing the roughness of the planarizing surface on the polishing pad, the rate of increase of the dishing or erosion of the remaining structure is decreased. In the preferred embodiment, the rate of dishing of a copper film is decreased with respect to tantalum and silicon dioxide films through the use of polishing pads exhibiting low levels of surface roughness.

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METHOD TO DECREASE DISHING RATE DURING CMP IN METAL SEMICONDUCTOR STRUCTURES

This application claims the benefit of Provisional Patent Application Serial No. 60/108,936 filed on November 18, 1998.

BACKGROUND OF THE INVENTION

Field of the Invention

The invention described in this patent pertains to the polishing and planarization of semiconductor structures by chemical-mechanical planarization (CMP), particularly those structures containing a metal, a barrier layer, and an insulating layer.

Prior Art

Chemical/Mechanical Planarization (or polishing), or CMP, is a powerful technology that has been instrumental in the semiconductor industry to enable the removal/planarization of thin films during the production of integrated circuits. Initial applications of this technology focused on the planarization of dielectric films such as SiO_2. However, as CMP becomes more widely adopted, the technology is being applied to more varied and complex structures: for example, the polishing of metal interconnect structures is becoming more widely accepted.

One type of structure that is increasingly more common involves inlaid metallic lines, sometimes referred to as damascene, or dual damascene, structures. The most common of these structures involves a metal conducting structure (typically composed of tungsten, aluminum, or copper) patterned into a dielectric film, typically composed of SiO_2. A barrier layer (typically composed of Ta, TaN, Ti, or TiN) exists between the metal and dielectric layers to inhibit migration of the metal film into the dielectric. When planarizing structures comprised of different film layers using CMP, it is desirable for the final structure to exhibit coplanarity with respect to each film. In the structure described above, the preferential removal of the metal layer with respect to the barrier or dielectric layer is typically referred to as "dishing" or "recess". Conversely, preferential removal of the dielectric layer with respect to it's initial film thickness or the metal layer is typically referred to as "erosion" or "oxide thinning".

One characteristic of the polishing process that can contribute to the unequal removal of different films within a semiconductor structure is the polishing slurry. Slurries containing different additives and abrasives, or exhibiting different chemical properties (i.e., pH), polish various films at different rates. For example, if a slurry removes the metal interconnect material faster than the dielectric material, the dishing or recess of the metal structure is possibly increased as a result. Additionally, the polishing process parameters (e.g., wafer downforce, platen rotational speed) can also have a strong influence on the final state of the semiconductor structure.

The effect of pad characteristics on the quality of a polishing process has also received a significant amount of attention. A number of different aspects of a pad have been specified as critical to produce a satisfactory semiconductor structure using CMP. For example, the elastic properties of a pad are known to be important to the planarization efficiency during CMP processes. Breivogel in U.S. Patent 5,212,910 present a composite pad structure made-up of three different materials that improves the ability of the pad to conform to the uneven surface of the film being polished. The chemical composition, structure, and make-up of pads used for polishing have also received much attention. Various pad structures have been specified, including urethane impregnated felts (U.S. Patent 4,927,432), polymeric matrices with impregnated void spaces (U.S. Patent 5,578,362) and solid polymeric materials (U.S. Patent 5,489,233).

One facet of polishing that has received little attention is the relationship of pad roughness to dishing, recess, and erosion of semiconductor structures. It is widely acknowledged that the texturing of the polishing pad is often necessary to achieve an adequate removal rate of the thin film being polished. In practice, this is typically done by continuously or semi-continuously abrading the surface of the pad during polishing. U.S. Patent 5,489,233 describes this as "microtexture which is produced by abrasion by a multiplicity of small abrasive points at a regular selected interval during the use of the pad". Typically, a diamond wheel is used as a source of "small abrasive points". However, the necessity of microtexture is described not in terms of pad roughness, but in terms of the

size of small flow channels in the pad, which are preferably "randomly oriented straight lines or grooves of randomly varying widths and depths". Additionally, no relationship to polishing performance is specified.

U.S. Patent 5,932,486 describes the roughness of the surface of pads used for chemical-mechanical polishing (CMP). It was determined that some pad surface roughness (about 0.1 microns) is necessary in CMP to obtain sufficient removal rates from the surface of semiconductor wafers.

SUMMARY OF THE INVENTION

A method is provided for polishing a composite semiconductor structure containing at least two different thin films, with the associated thin films exhibiting different removal rates. More preferably, a conducting metal interconnect layer, an insulating dielectric layer, and a barrier layer between the two: most preferably, a copper metal layer, a silicon dioxide dielectric layer, and a barrier layer of tantalum. The method comprises a polishing slurry that facilitates removal of at least one film preferentially with respect to the other films in said structure and a polishing pad containing a planarizing surface. By minimizing the roughness of the planarizing surface on the polishing pad, wherein the polishing pad has a planarizing surface with an average roughness less than 6 microns, and a root-mean square roughness less than 7 microns, the rate of dishing or erosion of the remaining structure is decreased. More preferably the pad has a planarizing surface with an average roughness less

than 4 microns, and a root-mean square roughness less than 5 microns. Even more preferably the polishing pad has a planarizing surface with an average roughness less than 2 microns, and a root-mean square roughness less than 2 microns. Most preferably the polishing pad has a planarizing surface with an average roughness less than 1 micron, and a root-mean square roughness less than 1 micron.

The method of this invention comprises contacting the substrate, which is comprised of at least two different materials, one of which is preferentially removed with respect to the other, with a polishing pad comprising a planarizing surface having an average roughness less than 6 microns, and a root-mean square roughness less than 7 microns, and effecting movement of the substrate and the planarizing surface relative to each other in the presence of a polishing composition that facilitates the removal of one of the materials at a faster rate than the other material.

Another aspect of the present invention is a polishing pad useful in chemical-mechanical polishing comprising a planarizing surface having an average roughness less than 6 microns, and a root-mean square roughness less than 7 microns.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

It has been found that a critical attribute of a polishing process used in the planarization of complex semiconductor structures is the surface roughness of the pad. In many CMP applications, it is desired to planarize

a structure containing films of two or more different materials. For example, a Cu interconnect structure contains barrier films of Ta or TaN, as well as an underlying dielectric film, typically SiO_2. To achieve a favorable final structure, it is desirable to have the Cu and SiO_2 films to be coplanar. One method to achieve this goal is to polish with slurries that have higher removal rates of Cu films with respect to the removal rates for either the barrier film (Ta or TaN) or the dielectric film (SiO_2).

However, even with slurries that exhibit high selectivities, it is common to remove some of the Cu layer below the plane of either the barrier layer or the dielectric layer. One possible cause of this phenomena is uncontrolled chemical etching by the polishing slurry. If the rate of removal of the film in question (i.e., Cu) is significant when no mechanical action is present, then regions of the semiconductor structure which are not in contact with the polishing surface will still exhibit removal. Therefore, it is desirable to design polishing slurries which demonstrate low static etch or corrosion potential with respect to the Cu (or metal) film. Another possible mechanism for the dishing of metal structures is pad deformation into the metal feature. If the removal rate of the surrounding dielectric film is low, these regions could act as a support to the polishing pad, allowing it to elastically deform into the metal structure and remove additional material. However, on the scale of features of concern in semiconductor structures (<1 micron to ~ 100 microns), it seems unlikely that this mechanism would contribute significantly.

In this patent, we have determined another source of dishing/erosion in CMP processes, namely the roughness of the polishing pad being used. In the structures described above, it has been found that the rate of dishing of a structure increases as the level of roughness of the polishing pad increases. This observation is consistent with a pad-asperity mechanism for polishing. In this model, the applied polishing load is transmitted to the piece being polished through individual asperities on the pad surface, therefore locally increasing the pressure associated with polishing. During the polishing of a patterned semiconductor structure, because of the difference in surface height of the polishing pad, the asperities can also extend into the metal feature, inducing dishing by contacting the recessed areas. The larger the size of the asperity, manifested as a rougher polishing surface, the more efficient the feature is at reaching into the recessed region, hence, the faster the rate of dishing of the metal line.

To quantify pad roughness, we have employed a stylus profilometer and measured average (Ra) and root mean square (Rq) roughness. Average roughness is defined as the average of the absolute values of the surface height variations measured from the mean surface level. Root-mean square roughness is defined as the square root of the mean value of the squares of the distances of the points from the mean surface level (Bennett and Mattsson, "Introduction to Surface Roughness and Scattering", Optical Society of America, Washington, DC, 1989, pp38-39). Any suitable technique for measuring surface roughness or the size of surface asperities could be employed: these include, but are not limited to, differential interference contrast microscopy, electron microscopy, atomic

force microscopy, scanning tunneling microscopy, and optical interferometry. Also, while average and root mean square roughness are commonly used measures of roughness, any parameter or appropriate surface statistic suitable to indicate the level of surface roughness could be used: these include, but are not limited to, peak-to-valley measurements, ten-point height, root-mean-square slope, parameters associated with surface height distribution functions, such as skewness and kurtosis, surface spatial wavelength, and parameters associated with the power-spectral-density function.

As described above, one typical semiconductor structure that could be polished using this method is comprised of a metal interconnect layer of copper, a barrier layer of tantalum, and a dielectric layer of silicon dioxide. With this structure, the method described above could be applied in at least two separate points in the structure. First, when using a slurry that has a high selectivity to copper vs. tantalum and silicon dioxide, at the point where the copper overburden is removed and the tantalum barrier layer is reached, this method can be applied to reduce the rate of dishing of the copper metalization structure (this case is covered in the examples below). Additionally, when using a slurry that has a high selectivity of copper and tantalum to silicon dioxide, at the point where the copper and tantalum overburden is removed and the silicon dioxide dielectric is reached, this method can also be applied to reduce the rate of dishing of the copper structure. However, it should be noted that this method is applicable to any semiconductor structure comprised of two or more materials where one is preferentially removed with respect to the other

during polishing. Also, it should be noted that this method is applicable in the case of multiple films when one film is preferentially removed with respect to numerous other films, or when numerous films are preferentially removed with respect to at least one other film.

It should also be noted that this method applies to *in situ* preferential removal of films in a semiconductor structure. For example, in a structure where the removal rates of a metal and the surrounding barrier metal are roughly equal, dishing of the metal may also be observed due to other effects in the polishing process (i.e., pattern density effects, galvanic effects, etc.). In the most general embodiment, this method is applicable when any differential film removal is observed on a semiconductor structure, and will decrease the rate of removal of any film that is preferably removed with respect to other films.

EXAMPLE

200 mm wafers with various surface films were polished on a IPEC/WESTECH 372U. An IC1000 polishing pad was used with an aqueous based slurry formulation comprising: water, a submicron abrasive, an oxidizing agent, and a surfactant or compound which acts to suppress the rate of removal of the dielectric insulating layer. Potassium hydroxide is used to adjust the pH to about 2 to 3. Polishing conditions were as follows: 5 psi downforce, 40 rpm carrier rotation, 1 psi backpressure, 150 ml/min slurry flowrate. The removal rates on various sheet wafers

(average of three wafers) is shown in Table 1 along with the resulting selectivities.

Table 1

Cu RR	Ta RR	SiO_2 RR	Cu:Ta	Cu:SiO_2
2757	70	16	39:1	172:1

Cu patterned wafers from SEMATECH (Austin, Texas) were polished on the machine and under the conditions as mentioned above. The Cu patterned wafers contain 8000 A deep features of various widths and configurations. A 500 A layer of Ta functions as a barrier layer between the Cu and underlying SiO_2 dielectric layer. Four different wafers were polished. Each wafer was polished with either an OXP3000 pad or an IC1000 pad (both manufactured by Rodel, Inc., Newark, DE). The pads used for sample 1 and 4 were used without any pre-conditioning (i.e., roughening of the surface using a diamond wheel for abrasion). For sample 2, the pad was conditioned with water and a diamond conditioning wheel for 10 minutes (20 pre-sweeps, 2 sweeps/min, platen speed = 75 rpm, 7 psi downforce). For sample 3, the pad was conditioned with water and a diamond conditioning wheel for 20 minutes (20 pre-sweeps, 2 sweeps/min, platen speed = 75 rpm, 7psi downforce). Polishing conditions were as follows: 5 psi downforce, 40 rpm carrier rotation, 1 psi backpressure, 150 ml/min slurry flowrate.

TABLE 2

Sample	Figure	Pad	Preconditioned?
1	1	OXP3000	No
2	2	IC1000	Yes
3	3	OXP3000	Yes
4	4	IC1000	No

The dishing/recess on two features (a 12 micron line and a 115x115 micron bond pad) were monitored at the center and edge of the wafer (four features total) at 30-45 second polishing intervals. Dishing/recess of the wafers was measured using a Tencor P-1 profilometer. The profilometer settings for the 115 micron pad were as follows: scan length = 0.3 mm, scanning speed = 0.01 mm/sec, stylus force = 15 milligrams, and stylus radius = 1.5 microns. The profilometer settings for the 12 micron line were as follows: scan length = 0.05 mm, scanning speed = 0.005 mm/sec, stylus force = 15 milligrams, and stylus radius = 1.5 microns. The data generated from the four trials described in Table 2 from the 12 micron feature at the wafer center are presented in Figures 1-4.

Initially, due to the underlying damascene structures (i.e., trenches, pads, and lines), the surface is non-planar, and 5000-6500 A of dishing (also referred to as step height) is present. As polishing proceeds, the structures are gradually planarized, and after a certain polishing time, no dishing is observed. For a certain amount of time, no dishing is present as the final layers of Cu overburden are removed. When the Ta barrier layer is reached, due to the higher removal rate of Cu film vs. Ta, dishing of the

Cu features begins to increase. As the wafer is overpolished, the dishing increases at a different rate for each of the trials, as is shown in Table 3.

TABLE 3

Sample	Figure	Dishing Rate - 12 micron feature (A/second)	Dishing Rate - 115 micron feature (A/second)
1	1	9.2	11.4
2	2	30.6	31.8
3	3	17.0	19.5
4	4	22.6	24.9

Post measurement of the four polishing pads with a Tencor P-1 profilometer after completion of the test was also conducted. Average roughness (Ra) and root-mean square roughness (Rq) were measured. The roughness values for each pad are given in Table 4.

TABLE 4

Sample	Figure	Average roughness (microns)	Root-mean square roughness (microns)
1	1	0.242	0.358
2	2	5.29	6.37
3	3	1.34	1.75
4	4	3.12	4.07

Based on the results shown above, the rate of dishing/recess after clearing the Cu from the wafer increases as the roughness of the pad

increases (See Figure 5). Therefore, to improve (i.e., increase) the process overpolish window, a pad with low roughness is desired.

Metal layers for which the process and slurries of this invention might be useful include, but are not limited to, tungsten, aluminum, copper, platinum, palladium, gold, iridium and any combination or alloy thereof.

Barrier layers for which the process and slurries of this invention might be useful include, but are not limited to, tantalum, tantalum nitride, titanium, titanium nitride, and any combinations thereof.

Insulating or dielectric layers for which the process and slurries of this invention might be useful include, but are not limited to, PSG, BPSG, TEOS, SiO_2, and any low-K polymeric material.

Depending on the chemicals used, the slurries of this invention may have a pH anywhere in the acidic, neutral, or alkaline range.

While specific embodiments of this invention have been shown above, the scope of this invention is defined by the claims which follow.

CLAIMS

1. A method for the chemical-mechanical polishing of a semiconductor substrate, which comprises,

contacting said substrate, which is comprised of at least two different materials, one of which is preferentially removed with respect to the other,

with a polishing pad comprising a planarizing surface having an average roughness less than 6 microns, and a root-mean square roughness less than 7 microns, and

effecting movement of said substrate and said planarizing surface relative to each other in the presence of a polishing composition that facilitates the removal of one of the materials at a faster rate than the other material.

2. The method of claim 1 wherein said polishing pad comprises a planarizing surface having an average roughness less than 4 microns, and a root-mean square roughness less than 5 microns.

3. The method of claim 1 wherein said polishing pad comprises a planarizing surface having an average roughness less than 2 microns, and a root-mean square roughness less than 2 microns.

4. The method of claim 1 wherein said polishing pad comprises a planarizing surface having an average roughness less than 1 micron, and a root-mean square roughness less than 1 micron.

5. The method of claim 1 wherein the substrate material that is removed at said faster rate is a conducting material and the other is a barrier material.

6. The method of claim 1 wherein the substrate material that is removed at said faster rate is a conducting material and the other is a dielectric material.

7. The method of claim 1 wherein the substrate material that is removed at said faster rate is a conducting material and the other material comprises both a barrier material and a dielectric material.

8. The method of claim 5 wherein said conducting material is from the group consisting of tungsten, aluminum, copper, platinum, palladium, gold, iridium and any combination or alloy thereof.

9. The method of claim 6 wherein said conducting material is from the group consisting of tungsten, aluminum, copper, platinum, palladium, gold, iridium and any combination or alloy thereof.

10. The method of claim 7 wherein said conducting material is from the group consisting of tungsten, aluminum, copper, platinum, palladium, gold, iridium and any combination or alloy thereof.

11. The method of claim 5 wherein said barrier material is from the group consisting of tantalum, tantalum nitride, titanium, titanium nitride, and any combinations thereof.

12. The method of claim 7 wherein said barrier material is from the group consisting of tantalum, tantalum nitride, titanium, titanium nitride, and any combinations thereof.

13. The method of claim 6 wherein said dielectric material is from the group consisting of PSG, BPSG, TEOS, SiO_2, and any low-K polymeric material.

14. The method of claim 7 wherein said dielectric material is from the group consisting of PSG, BPSG, TEOS, SiO_2, and any low-K polymeric material.

15. A polishing pad useful in chemical-mechanical polishing comprising a planarizing surface having an average roughness less than 6 microns, and a root-mean square roughness less than 7 microns.

16. A polishing pad according to claim 15 wherein said planarizing surface has an average roughness less than 4 microns, and a root-mean square roughness less than 5 microns.

17. A polishing pad according to claim 15 wherein said planarizing surface has an average roughness less than 2 microns, and a root-mean square roughness less than 2 microns.

18. A polishing pad according to claim 15 wherein said planarizing surface has an average roughness less than 1 micron, and a root-mean square roughness less than 1 micron.

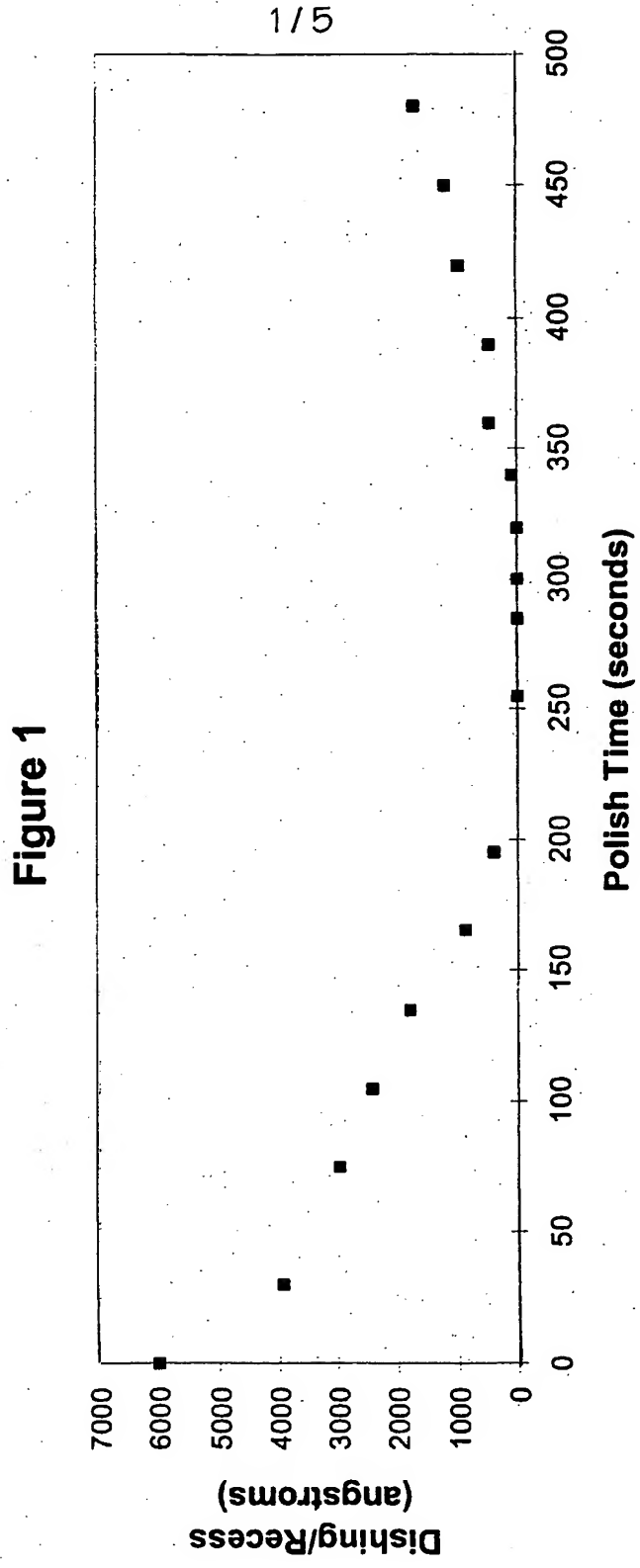
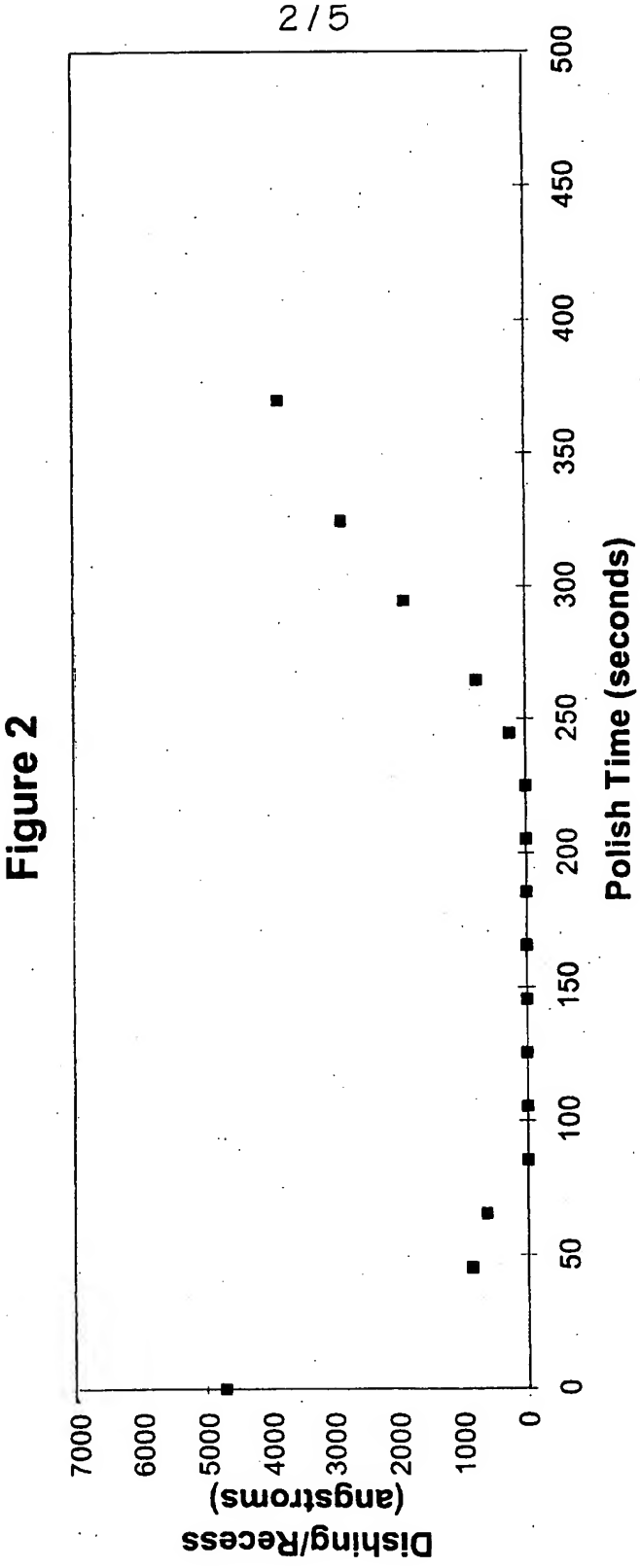

Dishing/Recess
(angstroms)
7000
6000
5000
4000
3000
2000
1000
0
Polish Time (seconds)
0
50
100
150
200
250
300
350
400
450
500

Figure 1


Dishing/Recess
(angstroms)
7000
6000
5000
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Polish Time (seconds)
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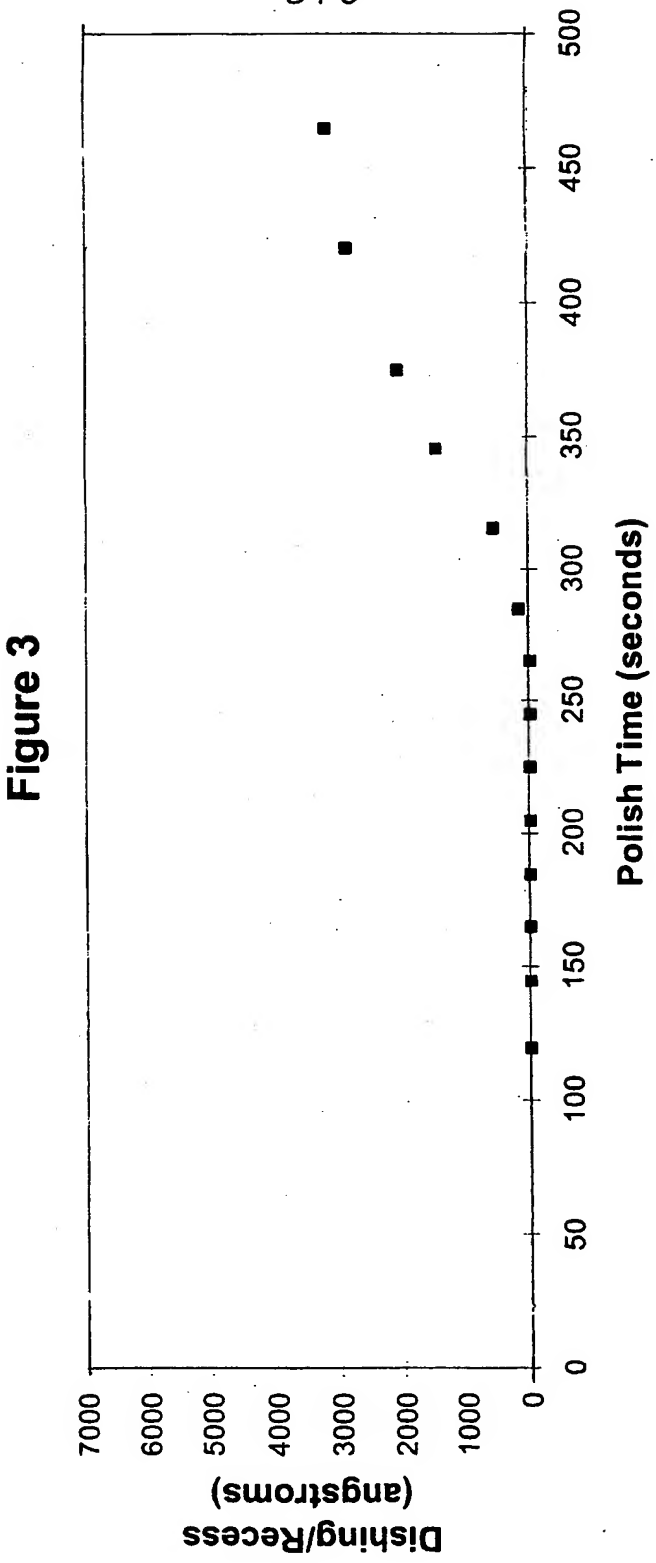
100
150
200
250
300
350
400
450
500

Figure 2


Dishing/Recess
(angstroms)
7000
6000
5000
4000
3000
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1000
0
Polish Time (seconds)
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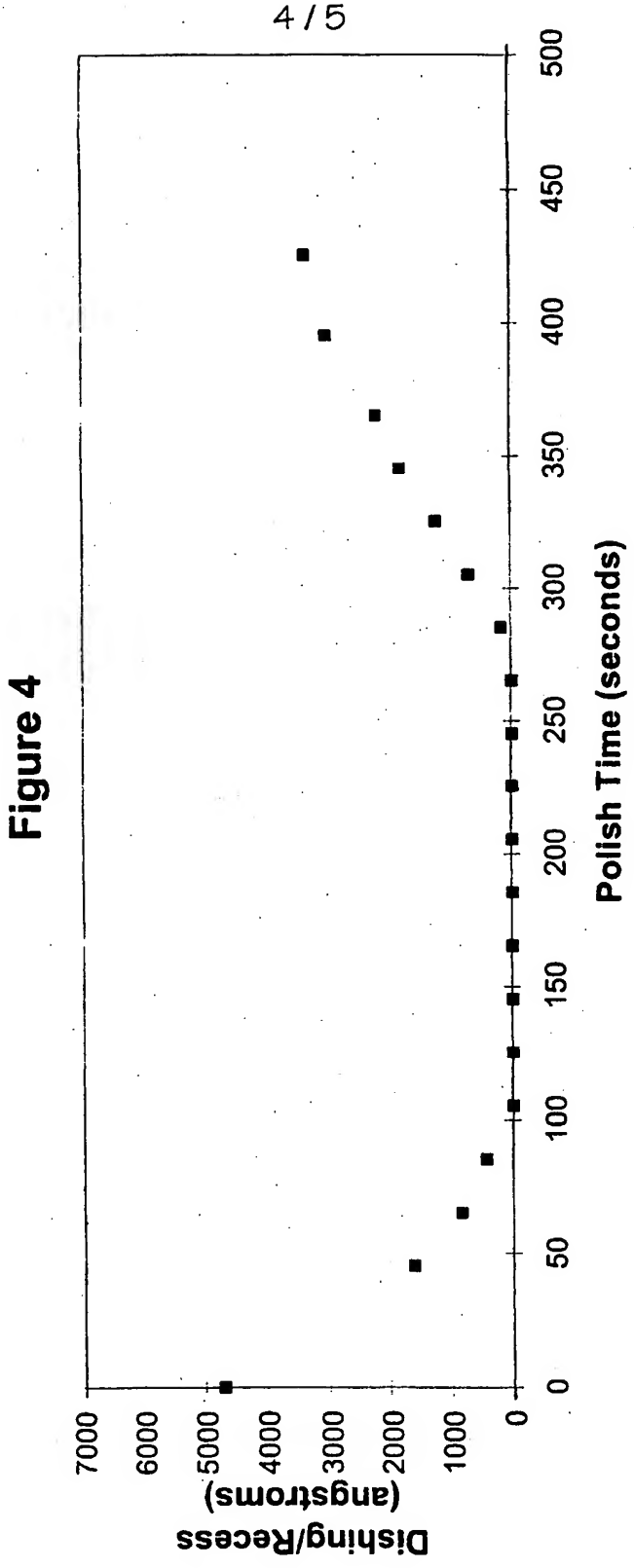
100
150
200
250
300
350
400
450
500

Figure 3


Dishing/Recess (angstroms)
7000
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5000
4000
3000
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Polish Time (seconds)
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50
100
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200
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300
350
400
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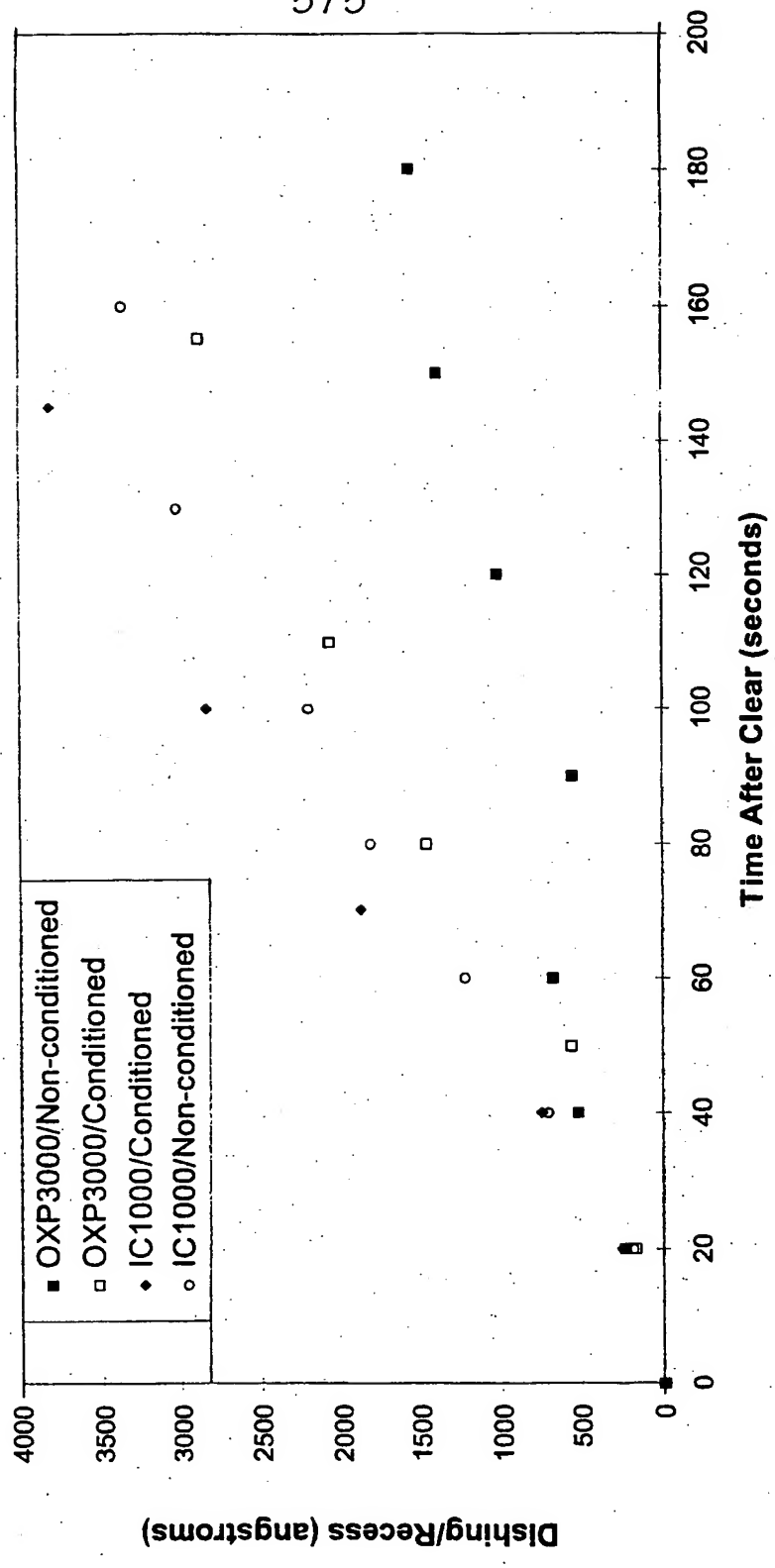
500

Figure 4


Dishing/Recess (angstroms)
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3500
3000
2500
2000
1500
1000
500
0
0
20
40
60
80
100
120
140
160
180
200
Time After Clear (seconds)
OXP3000/Non-conditioned
OXP3000/Conditioned
IC1000/Conditioned
IC1000/Non-conditioned

Figure 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/27225

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 21/00, 21/461, 21/4763; B24B 1/00, 7/24, 7/00
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/692, 645; 437/225; 451/41, 57, 59, 921; 216/88, 89; 156/636.1, 345

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y, P	US 5,932,486 A (**COOK ET AL.**) 03 August 1999, See col. 4, line 65 bridging to col. 5, line 5.	15-18
Y	US 5,096,854 A (**SAITO ET AL.**) 17 May 1992, See col. 2, line 65 bridging to col. 3, line 30.	15-18
A, P	US 5,985,755 A (**BAJAJ ET AL.**) 16 November 1999, See col. 4, lines 25-30.	1-18
A, P	US 5,916,011 A (**KIM ET AL.**) 29 June 1999, See col. 3, lines 63-67.	1-18
A, P	US 5,913,712 A (**MOLINAR**) 22 June 1999.	1-14
A	US 5,676,587 A (**LANDERS ET AL.**) 14 October 1997, col. 4, lines 5-11.	1-14

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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Date of the actual completion of the international search 24 MARCH 2000	Date of mailing of the international search report 18APR2000
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/27225

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,628,862 A (YU ET AL.) 13 May 1997, See col. 5, line 65 bridging to col. 6, line13.	1-14

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER:
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438/692, 645; 437/225; 451/41, 57, 59, 921; 216/88, 89; 156/636.1, 345